

CLAIMS

1
2 1. A current mode transfer logic transmission line driver system comprising:
3 a transmission line, defining at least a first and a second signal carrying conduc-
4 tor, the transmission line defining a characteristic impedance,
5 means for selectively driving unequal currents through the first and the second
6 signal carrying conductors, respectively,
7 a terminating resistor connected between the distal ends of the first and the second
8 signal carrying conductors,
9 means for receiving currents at the distal end of each transmission line, wherein
10 the received currents are unequal to each other, and
11 means for sensing the unequal currents.

1 2 The current mode transfer logic transmission line driver system of claim 1
2 wherein the means for selectively driving unequal currents through the two transmission
3 lines, comprises:
4 a first current source selectably connected to the first signal carrying conductor,
5 and
6 a second current source selectably connected to the second signal carrying con-
7 ductor of the first transmission line, the first and the second current sources of unequal
8 magnitudes.

1 3. The current mode transfer logic transmission line driver system of claim 1
2 wherein the means for receiving currents at the distal end of each transmission line com-
3 prises:
4 a first current receiving circuit connected between the distal end of the first
5 transmission line and at least one return path conductor, and
6 a second current receiving circuit connected between the distal end of the second
7 transmission line and at least one return path conductor.

1 4. The current mode transfer logic transmission line driver system of claim 1
2 wherein the first and the second current receiving circuits comprises diode connected
3 MOS transistors.

1 5. The current mode transfer logic transmission line driver system of claim 4 further
2 comprising means for biasing each diode connected MOS transistor so that it presents a
3 low impedance at the distal ends of the transmission lines, but wherein that low imped-
4 ance is substantially higher than the line's characteristic impedance.

1 6. The current mode transfer logic line driver system of claim 1 wherein the means
2 for sensing the unequal currents comprises means for comparing the currents in the first
3 receiving circuit to the current in the second receiving circuit.

1 7. The current mode transfer logic line driver system of claim 6 wherein the means
2 for comparing the currents in the first receiving circuit to the current in the second re-
3 ceiving circuit comprises:
4 a differential current amplifying circuit that amplifies the difference in the currents in the
5 first and the second receiving circuits.

1 8. The current mode transfer logic line driver system of claim 6 wherein the differ-
2 ential current amplifying circuit comprises:
3 a first amplifying current mirroring circuit providing an first output current,
4 a second amplifying current mirroring circuit providing a second output current,
5 and
6 a current to voltage conversion circuit, arranged to receive the first and the second output
7 currents and provides a voltage output that is proportional to the difference between the
8 outputs of the first and the second amplifying current mirroring circuits.

1 9. The current mode transfer logic transmission line driver system of claim 1
2 wherein the transmission line comprises:

3 a first transmission line defining the first signal carrying conductor and a charac-
4 teristic impedance with respect to at least one return path conductor,
5 a second transmission line defining the second signal carrying conductor and a
6 characteristic impedance with respect to at least one return path conductor,
7 wherein the at least one return path conductor is connected to ground.

1 10. A method for transferring current mode logic signals over transmission lines
2 comprising the steps of:
3 defining a transmission line with at least a first and a second signal carrying con-
4 ductor,
5 defining a characteristic impedance with respect to the at least first and second
6 signal carrying conductors,
7 selectively driving unequal currents through the two signal carrying conductors,
8 providing a terminating resistor between the distal ends of the at least first and the
9 second signal carrying conductors,
10 receiving currents from the distal end of the transmission line, wherein the re-
11 ceived currents are unequal to each other, and
12 sensing the unequal currents.

1 11 The method for transferring current mode logic signals of claim 9 wherein the
2 selectively driving unequal currents through the two signal carrying conductors, com-
3 prises the steps of:
4 selectably connecting a first current source to the first signal carrying conductor,
5 and
6 selectively connecting a second current source to the second signal carrying con-
7 ductor, wherein the first and the second current sources are of unequal magnitudes.

1 12. The method for transferring current mode logic signals of claim 10 wherein the
2 receiving currents from the distal end of the transmission line comprises the steps of:

3 receiving a first current from the distal end of the first signal carrying conductor,
4 and
5 receiving a second current from the distal end of the second signal carrying con-
6 ductor.

1 13. The method for transferring current mode logic signals of claim 12 wherein the
2 first and the second currents are received by diode connected MOS transistors.

1 14. The method for transferring current mode logic signals of claim 13 further com-
2 prising the steps of biasing each diode connected MOS transistor so that it presents a low
3 impedance at the distal ends of the transmission lines, but wherein that low impedance is
4 substantially higher than the line's characteristic impedance.

1 15. The method for transferring current mode logic signals of claim 10 wherein the
2 step of sensing the unequal currents comprises the step of comparing the current in the
3 first receiving circuit to the current in the second receiving circuit.

1 16. The method for transferring current mode logic signals of claim 15 wherein the
2 step of comparing the currents in the first receiving circuit to the current in the second
3 receiving circuit comprises the step of amplifying the difference in the currents in the first
4 and the second receiving circuits.

1 17. The method for transferring current mode logic signals of claim 15 wherein the
2 step of amplifying the difference comprises the steps of:
3 first mirroring and amplifying the current in the first receiving circuit and pro-
4 viding an first output current,
5 second mirroring and amplifying the current in the first receiving circuit and pro-
6 viding a second output current,
7 receiving the first and the second output currents, and

8 provides a voltage output that is proportional to the difference between the re-
9 ceived first and the second output currents.

1 18. The method for transferring current mode logic signals of claim 10 wherein the
2 step of defining a transmission line comprises the steps of:
3 defining a first transmission line having the first signal carrying conductor and a
4 characteristic impedance with respect to at least one return path conductor, and
5 defining a second transmission line having the second signal carrying conductor
6 and a characteristic impedance with respect to at least one return path conductor,
7 wherein the at least one return path conductor is connected to ground.